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14. ABSTRACT
In this project, work has been performed on nine different topics: (1) Ultra-fast microwave annealing of ion-implanted 4H-SiC ; (2) Silicon carbide nanowires grown by a novel microwave heating-assisted physical vapor transport process; (3) Depth resolved X-ray determination of surface strain in free-standing films of HVPE-grown GaN and 71Ga NMR characterization (4) Effects of the surface and interface related defects in free-standing HVPE grown GaN films by high resolution X-ray diffraction measurements; (5) Bias stress induced instability in 4H-SiC DMOSFETs; (6) Stability and 2-D simulation studies of avalanche breakdown in 4H-SiC DMOSFETs with JTE; and (7) Power added efficiency and linearity tradeoffs in class AB biased GaN

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Report Title

ABSTRACT

In this project, work has been performed on nine different topics: (1) Ultra-fast microwave annealing of ion-implanted 4H-SiC ; (2) Silicon carbide nanowires grown by a novel microwave heating-assisted physical vapor transport process; (3) Depth resolved X-ray determination of surface strain in free-standing films of HVPE-grown GaN and 71Ga NMR characterization (4) Effects of the surface and interface related defects in free-standing HVPE grown GaN films by high resolution X-ray diffraction measurements; (5) Bias stress induced instability in 4H-SiC DMOSFETs; (6) Stability and 2-D simulation studies of avalanche breakdown in 4H-SiC DMOSFETs with JTE; and (7) Power added efficiency and linearity tradeoffs in class AB biased GaN and GaAs microwave power HEMTs (8) High quality interlayer dielectric for 4H-SiC DMOSFETs; and (9)Thermally stable Ge/Cu/Ti ohmic contacts to n-type GaN. Important results on each topic are given in the attachment. We collaborated with Dr. Ken Jones of ARL on the topic: microwave annealing of implanted SiC .

List of papers submitted or published that acknowledge ARO support during this reporting period. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

1.S. G. Sundaresan, M. V. Rao, Y-L. Tian, J. A. Schreifels, M. C. Wood,and K. A. Jones, "Comparison of solid-state microwave annealing with conventional furnace annealing of ion-implnted SiC", Journal of Electronic Materials, Vol. 36, pp. 324-331 (2007).

2. S. G. Sundaresan, M. V. Rao, Y-L. Tian, M. C. Ridgway, J. A. Schreifels and J. J. Kopanski, "Ultra-high-temperature microwave annealing of Al+- and P+-implanted 4H-SiC", Journal of Applied Physics, Vol. 101,0737081(1-7) (2007) .

3. S. G. Sundaresan, Y-L. Tian, M. C. Ridgway, N. A. Mahadik, S. B. Qadri, and M. V. Rao, "Solid-state microwave annealing of ion-implanted 4H-SiC", Nuclear Instruments and Methods in Physics Research, Vol. B 261, pp. 616-619 (2007).

4. S. G. Sundaresan, N. Mahadik, S.B. Qadri, J. A. Schreifels , Y-L. Tian, Q. Zhang, E. Gomar-Nadal, M.V. Rao, "Ultra-low resistivity Al-implanted 4H-SiC obtained by high-temperature rapid microwave annealing and a protective graphite cap", Solid-State Electronics, in press.

5. S. G. Sundaresan, A. V. Davydov, M. Vaudin, J. Maslar, I. Levin, J. Schlager, Y-L. Tian, M. V. Rao, "Silicon carbide nanowires grown by a microwave heating-assisted physical vapor transport process", Chemistry of Materials, in press.

6. N. Mahadik, S.B. Qadri, M.V. Rao and J.P. Yesinowski, "Depth resolved X-ray determination of surface strain in free-standing films of HVPE-grown GaN and 71Ga NMR characterization", Applied Physics A, Vol. 86, pp. 67-71 (2007).

7. N. A. Mahadik, S. B. Qadri, and M.V. Rao, "Effects of the surface and interface related defects in free-standing HVPE grown GaN films by high resolution X-ray diffraction measurements", Thin Solid Films, in press.

8. T. Okayama, S. D. Arthur, J. L. Garrett, and M. V. Rao, "Bias stress induced instability in 4H-SiC DMOSFETs", Solid-State Electronics, in press.

9. T. Okayama, S.D. Arthur, and M. V. Rao, "High quality interlayer dielectric for 4H-SiC DMOSFETs", Semiconductor Science and Technology, in press.

10. N Mahadik, M. V. Rao and A. V. Davydov, "Thermally stable Ge/Cu/Ti ohmic contacts to n-type GaN", Journal of Electronic Materials, Vol. 35, 2035-2040 (2006).

Number of Papers published in peer-reviewed journals: 10.00

(b) Papers published in non-peer-reviewed journals or in conference proceedings (N/A for none)

Number of Papers published in non peer-reviewed journals: 0.00

(c) Presentations

(1) S.G. Sundaresan et. al, "Solid-state microwave annealing of ion-implanted SiC", 16th International Conference on "Ion-Beam Modification of Materials (IBMM), Taormina, Italy, September 18-22, 2006

(2)N.A. Mahadik, S.B. Qadri, M. Murthy, M.V. Rao, J. Freitas, "Double-Crystal X-Ray Topography of Free-Standing HVPE Grown n-type GaN",International Conference on Metallurgical Coatings and Thin Films, San Diego, CA, April 23-27, 2007

(3) S.G. Sundaresan, A.V. Davydov, M. Vaudin, I. Levin, Y-L. Tian, M.V. Rao, N. Sanford, T. Robbins, "A novel microwave based technique for rapid and controllable growth of SiC nanowires", Nanotech 2007 Conference (NSTI Bio Nano 2007),Santa Clara, CA, May 20-24, 2007.

(4) T. Okayama, S.D. Arthur, J.L. Garrett, M.V. Rao, "Reliability of 4H-SiC DMOSFETs evaluated by bias stressing", Device Research Conference 2007, Univ. of Notre Dame, IN, June 18-20, 2007

(5) S. G. Sundaresan, A.V. Davydov, M.D. Vaudin, I.E. Levin, J.E. Maslar, Y-L. Tian, M.V. Rao, "Growth of SiC nanowires by a novel microwave-assisted vapor transport process", Nanoelectronic Devices for Defense and Security Conference, Crystal City, VA, June 18-21, 2007

(6) S.G. Sundaresan, Y-L. Tian, J.A. Schriefels, N.A. Mahadik, S.B. Qadri, E. Gomar-Nadal, E.D. Williams, J. Zhang, M.V. Rao, "Ultra-low resistivity Al-implanted SiC obtained by microwave annealing and a protective graphite cap", 49 th Electronic Materials Conference, Univ. of Notre Dame, June 20-22, 2007.

(7) S.G. Sundaresan et. al, "A study of AlN and MgO caps for protecting the GaN surface during ultra-fast microwave annealing", 49th Electronic Materials Conference, Univ. of Notre Dame, IN, June 20-22, 2007.

(8) N. Mahadik, M.V. Rao, and A.V. Davydov, "Ge/Cu/Ti ohmic contacts to n-type GaN", 2005 International Semiconductor Device Research Symposium, December 4-6, 2005.

(9) N. Mahadik, M.V. Rao, S.B. Qadri, and J.P. Yesinowski, "Structural characteristics of hydride vapor phase epitaxy grown GaN",2005 International Semiconductor Device Research Symposium, December 4-6, 2005.

Number of Presentations: 9.00

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Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts): 0

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts): 0

(d) Manuscripts

(1) T. Okayama, S.D. Arthur, R. Rao, K. Kishore, M.V. Rao, "Stability and 2-D simulation studies of avalanche breakdown in 4H-SiC DMOSFETs with JTE", IEEE Transactions on Electron Devices.

Number of Manuscripts: 1.00

Number of Inventions:

Graduate Students

NAME	PERCENT_SUPPORTED
Nadeemullah Mahadik	0.25
Taizo Okayama	0.20
Siddarth Sundaresan	0.25
FTE Equivalent:	**0.70**
Total Number:	**3**

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Mulpuri, V. Rao	0.15	No
FTE Equivalent:	**0.15**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	0.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):	0.00
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The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	0.00

Names of Personnel receiving masters degrees

NAME
Total Number:

Names of personnel receiving PHDs

NAME
Siddarth Sundaresan, October 2007
Taizo Okayama, November 2007
Nadeemullah Mahadik, December 2008
Total Number: 3

Names of other research staff

NAME	PERCENT SUPPORTED
FTE Equivalent:	
Total Number:	

Sub Contractors (DD882)

Inventions (DD882)

FINAL REPORT

Award # W911NF-04-1-0428
Project Name: Defects and Related Carrier Traps in GaN/AlGaN and implanted SiC
Performance Period: September 15, 2004 – September 14, 2007

Abstract:

In this project work has been performed on nine different topics: (1) Ultra-fast microwave annealing of ion-implanted 4H-SiC ; (2) Silicon carbide nanowires grown by a novel microwave heating-assisted physical vapor transport process; (3) Depth resolved X-ray determination of surface strain in free-standing films of HVPE-grown GaN and ^{71}Ga NMR characterization (4) Effects of the surface and interface related defects in free-standing HVPE grown GaN films by high resolution X-ray diffraction measurements; (5) Bias stress induced instability in 4H-SiC DMOSFETs; (6) Stability and 2-D simulation studies of avalanche breakdown in 4H-SiC DMOSFETs with JTE; and (7) Power added efficiency and linearity tradeoffs in class AB biased GaN and GaAs microwave power HEMTs (8) High quality interlayer dielectric for 4H-SiC DMOSFETs; and Thermally stable Ge/Cu/Ti ohmic contacts to n-type GaN. Abstracts on each topic are given in the detailed report. Important results on the above topics include: successful development of a novel microwave based technique for annealing ion-implanted SiC, which yielded material with excellent electrical and lattice quality; growth of cubic SiC nanowires using a simple microwave heating assisted sublimation sandwich method; evaluation of structural quality of HVPE grown fee standing GaN using non-destructive x-ray diffraction techniques; a thorough study on threshold voltage and breakdown voltage instability of 4H-SiC DMOSFETs caused by SiC/SiO2 interface charge trapping/detrapping; a comparative study on the power and linearity characteristics of GaN/AlGaN HEMT and psuedomorphic GaAs HEMT devices; and developing optimum boron and phosphorus percentage concentrations in borophosphosilicate glass dielectric encapsulants for DMOS applications; and finding optimum Cu-Ge-Ti based ohmic contact processing conditions for n-type GaN. We collaborated with Dr. Ken Jones of ARL on the topic: microwave annealing of implanted SiC .

(1) Ultra-fast microwave annealing of ion-implanted 4H-SiC

In this work, an ultrafast solid-state microwave annealing was performed, in the temperature range of 1700–2120 °C on Al^+- and P^+-implanted 4*H*-SiC. The solid-state microwave system used in this study is capable of raising the SiC sample temperatures to extremely high values, at heating rates of ≈ 600 °C/s. The samples were annealed for 5–60 s in a pure nitrogen ambient. Atomic force microscopy performed on the annealed samples indicated a smooth surface with a rms roughness of 1.4 nm for 5×5 μm^2 scans even for microwave annealing at 2050 °C for 30 s. Auger sputter profiling revealed a <7 nm thick surface layer composed primarily of silicon, oxygen, and nitrogen for the samples annealed in N_2, at annealing temperatures up to 2100 °C. X-ray photoelectron

spectroscopy revealed that this surface layer is mainly composed of silicon oxide and silicon nitride. Secondary ion mass spectrometry depth profiling confirmed almost no dopant in diffusion after microwave annealing at 2100 °C for 15 s. However, a sublimation of ~100 nm of the surface SiC layer was observed for 15 s annealing at 2100 °C. Rutherford backscattering spectra revealed a lattice damage-free SiC material after microwave annealing at 2050 °C for 15 s, with scattering yields near the virgin SiC material. Van der Pauw–Hall measurements have revealed sheet resistance values as low as 2.4 kΩ/□ for Al^+-implanted material annealed at 2100 °C for 15 s and 14 Ω/□ for the P^+-implanted material annealed at 1950 °C for 30 s. The highest electron and hole mobilities measured in this work were 100 and 6.8 cm^2/V s, respectively, for the P^+- and Al^+-implanted materials.

In order to eliminate surface sublimation, we have employed a graphite cap for rapid microwave annealing of aluminum implanted 4H–SiC, in the temperature range of 1750–1900 °C, for 30 s durations. The graphite cap prevailed even for 1900 °C/30 s microwave annealing yielding a low surface roughness of 2.4 nm. Rutherford backscattering-channeling spectra indicated that 1900 °C microwave annealing is much more effective than 1800 °C/5 min conventional furnace annealing in not only alleviating the implantation-induced lattice damage but also in removing some of the defects introduced during growth of the 4H–SiC epi-layer used for the Al^+ implantation. Van der Pauw–Hall measurements indicated an extremely low sheet resistance of 2.8 kΩ/□ for the 1900 °C/30 s annealing, which is about 5 times smaller than the sheet resistance measured on the 1800 °C/ 5 min conventional furnace annealed material.

Publications on this topic acknowledging the Award:

1.S. G. Sundaresan, M. V. Rao, Y-L. Tian, J. A. Schreifels, M. C. Wood,and K. A. Jones, “Comparison of solid-state microwave annealing with conventional furnace annealing of ion-implnted SiC”, Journal of Electronic Materials, Vol. 36, pp. 324-331 (2007).

2. S. G. Sundaresan, M. V. Rao, Y-L. Tian, M. C. Ridgway, J. A. Schreifels and J. J. Kopanski, “Ultra-high-temperature microwave annealing of Al^+- and P^+-implanted 4H-SiC”, Journal of Applied Physics, Vol. 101,0737081(1-7) (2007) .

3. S. G. Sundaresan, Y-L. Tian, M. C. Ridgway, N. A. Mahadik, S. B. Qadri, and M. V. Rao, “Solid-state microwave annealing of ion-implanted 4H-SiC”, Nuclear Instruments and Methods in Physics Research, Vol. B 261, pp. 616-619 (2007).

4. S. G. Sundaresan, N. Mahadik, S.B. Qadri, J. A. Schreifels , Y-L. Tian, Q. Zhang, E. Gomar-Nadal, M.V. Rao, “Ultra-low resistivity Al-implanted 4H-SiC obtained by high-temperature rapid microwave annealing and a protective graphite cap”, Solid-State Electronics, in press.

(2) Silicon carbide nanowires grown by a novel microwave heating-assisted physical vapor transport process

SiC nanowires are grown by a novel catalyst-assisted sublimation-sandwich (SS) method. This involves microwave heating-assisted physical vapor transport from a *source* 4H-SiC wafer to a closely positioned *substrate* 4H-SiC wafer. The *substrate wafer* is coated with a group VIII (Fe, Ni, Pd, Pt) metal catalyst film about 5 nm thick. The nanowire growth is performed in a nitrogen atmosphere, in the temperature range of 1650 ºC to 1750 ºC for 40 s durations. The nanowires grow by the vapor-liquid-solid (VLS) mechanism facilitated by metal catalyst islands that form on the substrate wafer surface at the growth temperatures used in this work. The nanowires are 10 μm to 30 μm long. About 52% of the nanowires had diameters in the range of 15 nm – 150 nm, whereas 14% of the nanowires had diameters in excess of 300 nm. Electron backscatter diffraction (EBSD) and selected area electron diffraction (SAD) analyses confirmed nanowires to crystallize with a cubic 3C structure of 3C-SiC. EBSD from the nanowire caps were indexed as Fe_2Si, Ni_3Si, Pd_2Si, and PtSi phases for the nanowires grown using Fe, Ni, Pd, and Pt as the metal catalysts, respectively. The nanowires are found to grow along the ⟨112⟩ directions, as opposed to the commonly observed ⟨111⟩ directions. The μ-Raman spectra from single nanowires indicate regions with varying compressive strain in the nanowires and also shows modes not arising from the Brillouin zone-center, which may indicate the presence of defects in the nanowire.

Publications on this topic acknowledging the Award:

1. S. G. Sundaresan, A. V. Davydov, M. Vaudin, J. Maslar, I. Levin, J. Schlager, Y-L. Tian, M. V. Rao, "Silicon carbide nanowires grown by a microwave heating-assisted physical vapor transport process", Chemistry of Materials, in press.

(3) Depth resolved X-ray determination of surface strain in free-standing films of HVPE-grown GaN and ^{71}Ga NMR characterization

Free-standing GaN films grown by hydride vapor phase epitaxy (HVPE) on *c*-plane sapphire have been studied for in-plane anisotropic strain. Lattice parameters are obtained from high-resolution X-ray diffraction data and the film quality is determined by measuring the rocking curves and by 71Ga nuclear magnetic resonance (NMR). The in-plane strain was determined using grazing incidence X-ray diffraction and conventional Xray measurements. It is found that the in-plane lattice parameter varies with depth and has estimated surface strain anisotropy of $4.0791\times10-3$ up to a thickness of 0.3 μm. The 71Ga NMR experiments reveal different degrees of inhomogeneity amongst the three samples. This is shown by the appearance of an additional broad central-transition peak shifted to higher frequency by a Knight shift from conduction electrons in sample regions having high carrier concentrations.

Publications on this topic acknowledging the Award:

1. N. Mahadik, S.B. Qadri, M.V. Rao and J.P. Yesinowski, "Depth resolved X-ray determination of surface strain in free-standing films of HVPE-grown GaN and ^{71}Ga NMR characterization", Applied Physics A, Vol. 86, pp. 67-71 (2007).

(4) Effects of the surface and interface related defects in free-standing HVPE grown GaN films by high resolution X-ray diffraction measurements

High-resolution X-ray topography (HRXT) and rocking curve measurements were performed on unintentionally doped, freestanding HVPE grown n-type Gallium Nitride (GaN). Based on the rocking curve widths, the dislocation density is estimated to be in the range of 10^5–10^7/cm^2, and the lower limit of average crystallite sizes to be 340–500 nm normal to the surface of the film. The lateral dimensions of crystallites and cavities were obtained from HRXT images, and are estimated to be in 200–500 nm, and 0.5–400 μm ranges, respectively. Although the GaN films are freestanding, they are warped with a radius of curvature of about 0.5 m, as determined from topographic measurements. The warpage is attributed to thermal mismatch between GaN and the substrate during growth.

Publications on this topic acknowledging the Award:

1. N. A. Mahadik, S. B. Qadri, and M.V. Rao, "Effects of the surface and interface related defects in free-standing HVPE grown GaN films by high resolution X-ray diffraction measurements", Thin Solid Films, in press.

(5) Bias stress induced instability in 4H-SiC DMOSFETs

In this work, the instability of n-channel 4H-SiC double-implanted metal-oxide-semiconductor field-effect- transistors (DMOSFETs) were studied, in terms of threshold voltage (V_{TH}) shifts and drain-source current (I_{DS}) transients, for different gate bias stress durations of range 100 s – 5,500s. At room temperature, for positive gate bias stress, the V_{TH} shift and I_{DS} decay increase with increasing stress time. The V_{TH} shift and the I_{DS} decay were recovered by negative gate bias stress. It is believed that the instability in device behavior during positive gate bias stress is due to capture of electrons by the SiC/gate dielectric interface traps and the gate dielectric near interface traps. Elevated temperature measurements have indicated a decrease in V_{TH} and an increase in I_{DS} with increasing stress time possibly due to mobile positive ions in the gate dielectric.

Publications on this topic acknowledging the Award:

1. T. Okayama, S. D. Arthur, J. L. Garrett, and M. V. Rao, "Bias stress induced instability in 4H-SiC DMOSFETs", Solid-State Electronics, in press.

(6) Stability and 2-D simulation studies of avalanche breakdown in 4H-SiC DMOSFETs with JTE

In this work, the stability of n-channel 4H-SiC double-implanted metal-oxide-semiconductor field-effect- transistors (DMOSFETs) with junction termination extension (JTE) was assessed by measuring the breakdown voltage (BV) of these devices before and after bias stress at a high temperature. The BV slumped after the DMOSFET was bias stressed at 1,200 V for 2 hours at 175 °C, and the slumped BV dynamically recovered to the pre-stress value during the post-stress period. Computer simulation suggests that the BV-slump and its recovery are dominated by the charge trapping/detrapping phenomena at the SiC/field oxide interface in the JTE structure, rather than the trapping/detrapping at the SiC/gate oxide interface in the cell structure. A positive interface charge of approximately one-third of the sheet dopant concentration of the JTE region, lowers BV by 150 V, which is the typical measured BV-slump of the DMOSFETs of this study.

Publications on this topic acknowledging the Award:

1. T. Okayama, S.D. Arthur, R. Rao, K. Kishore, and M.V. Rao, "Stability and 2-D simulation studies of avalanche breakdown in 4H-SiC DMOSFETs with JTE", IEEE Transactions on Electron Devices, in review.

(7) Power added efficiency and linearity tradeoffs in class AB biased GaN and GaAs microwave power HEMTs

In this work, power-added efficiency (PAE) and linearity characteristics AlGaN/GaN HEMTs are compared with those high-voltage GaAs pseudomorphic HEMTs. Devices with different gate widths are characterized for their power output, gain, PAE and linearity performances as a function of bias current and source and load impedance. When compared to the source/load power matched condition, source tuning provides a significant improvement in the linearity without compromising the PAE performance, whereas, load tuning results in a substantial reduction in PAE to gain a marginal improvement in linearity. For the GaN devices, a maximum power-added efficiency (PAE) of 58.5 % for class AB operation and a maximum third-order intercept point (IP3) of 42.7 dBm for class A operation were obtained. When operated at similar dc power dissipation conditions under class-AB bias, similar output power and high-drive third-order inter-modulation (IM3) were measured for GaN and GaAs devices, but the power density is three times higher for the GaN devices.

Publications on this topic acknowledging the Award:

1. T. Okayama, J.A. Roussos, S. C. Binari, and M. V. Rao, "Power added efficiency and linearity tradeoffs in class AB biased GaN and GaAs microwave power HEMTs", Electronics Letters (in Preparation)

(8) High quality interlayer dielectric for 4H-SiC DMOSFETs

In this work useful weight percentages of boron and phosphorus in boro-phospho-silicate-glass (BPSG) interlayer dielectric (ILD) films to getter mobile ions effectively are developed, considering the limitations such as: required low glass flow temperature;

and possible hygroscopic nature of the films and formation of crystalline BPO_4 particles, which may occur for high B and P weight percentages. The B and P weight percentage viscous flow temperature contours and empirical inequalities representing the above mentioned limitations are developed and discussed. Results of this work are useful for both silicon and compound semiconductor device technologies.

Publications on this topic acknowledging the Award:

1. T. Okayama, S.D. Arthur, and M. V. Rao, "High quality interlayer dielectric for 4H-SiC DMOSFETs", Semiconductor Science and Technology, in press

(9) Thermally stable Ge/Cu/Ti ohmic contacts to n-type GaN

The performance of a novel Ge/Cu/Ti metallization scheme on n-type GaN has been investigated for obtaining thermally and electrically stable low-resistance ohmic contacts. Isochronal (2 min.) anneals in the 600–740°C temperature range and isothermal (690°C) anneals for 2–10 min. duration were performed in inert atmosphere. For the 690°C isothermal schedule, ohmic behavior was observed after annealing for 3 min. or longer with a lowest contact resistivity of 9.1 3 10_5 V cm2 after the 10 min. anneal for a net donor doping concentration of 9.2 3 1017 cm_3. Mean roughness (Ra) for anneals at 690°C was almost constant at around 5 nm, up to an annealing duration of 10 min., which indicates a good thermal stability of the contact scheme.

Publications on this topic acknowledging the Award:

1. N Mahadik, M. V. Rao and A. V. Davydov, "Thermally stable Ge/Cu/Ti ohmic contacts to n-type GaN", Journal of Electronic Materials, Vol. 35, 2035-2040 (2006).